



1st Korea–Vietnam Joint Workshop of Solid-State Circuits and Systems

January 25 and 26, 2016

**Meeting Room 2, 6th floor, Main Building,
University of Technology and Education,
Ho Chi Minh City, Vietnam**

Co-organized by

**Institute of Korean Electrical and Electronics Engineers (IKEEE), Korea
and**

**Department of Electrical and Electronics Engineering, University of
Technology and Education, HCMC, Vietnam (FEEE-HCMUTE)**



**INSTITUTE OF KOREAN
ELECTRICAL AND ELECTRONICS ENGINEERS**



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Kyeong-Sik Min (Kookmin University, Seoul, Korea)
Van Hieu Nguyen (University of Science, VNU, HCMC, Vietnam)
Minh Huan Vo (University of Technology and Education, HCMC, Vietnam)

INVITED SPEAKERS

Minkyu Song (Dongguk University, Seoul, Korea)
Jongsun Kim (Hongik University, Seoul, Korea)
Yong Moon (Soongsil University, Seoul, Korea)
Seongsoo Lee (Soongsil University, Seoul, Korea)
Kyeong-Sik Min (Kookmin University, Seoul, Korea)
Quang Vinh Ngo (ICDREC, HCMC, Vietnam)
Tuan Khanh Nguyen (ICDREC, HCMC, Vietnam)
Bach Thang Phan (University of Science, VNU, HCMC, Vietnam)
Hitoshi Sugihara (Renesas Design Vietnam, Co., Ltd., HCMC, Vietnam)
Minh Son Nguyen (University of Information Technology, HCMC, Vietnam)
Minh Huan Vo (University of Technology and Education, HCMC, Vietnam)



WORKSHOP PROGRAM

Tuesday, January 26, 2016	
08:50 AM - 09:20 AM	Poster session, Registration
09:20 AM - 09:30 AM	Opening address, Van Thuyen Ngo Vice President of University of Technology and Education, HCMC, Vietnam
09:30 AM - 09:50 AM	A full-swing 10-Bit CMOS cyclic D/A converter with a capacitor-sharing technique, Minkyu Song, Dongguk University, Seoul, Korea
09:50 AM - 10:10 AM	Low power SerDes for wireless chip-to-chip communication, Jongsun Kim, Hongik University, Seoul, Korea
10:10 AM - 10:30 AM	A study of mm-Wave circuits based on meta-material, Yong Moon, Soongsil University, Seoul, Korea
10:30 AM - 10:50 AM	Break
10:50 AM - 11:10 AM	Battery lifetime and PSNR quality-scalable video transmission for mobile multimedia systems, Seongsoo Lee, Soongsil University, Seoul, Korea
11:10 AM - 11:30 AM	Memristor crossbar circuits for energy-efficient pattern recognition, Kyeong-Sik Min, Kookmin University, Seoul, Korea
11:30 AM - 13:30 PM	Lunch
13:30 PM - 13:50 PM	A successful model in building-up the semiconductor industry at Vietnam, Hitoshi Sugihara, Renesas Design Vietnam, Co., Ltd., HCMC, Vietnam
13:50 PM - 14:10 PM	Study of the resistive switching effect in chromium oxide thin films by use of conductive atomic force microscopy, Bach Thang Phan, University of Science, VNU, HCMC, Vietnam
14:10 PM - 14:30 PM	A new multiplication architecture with mixed data format for DSP applications, Minh Son Nguyen, University of Information Technology, HCMC, Vietnam
14:30 PM - 14:50 PM	ICDREC and the development of IC design in Vietnam, Quang Vinh Ngo, ICDREC, HCMC, Vietnam
14:50 PM - 15:10 PM	Dual power gating techniques for small leakage energy loss in low power applications, Minh Huan Vo, University of Technology and Education, HCMC, Vietnam
15:10 PM - 15:30 PM	Break
15:30 PM - 15:50 PM	Introduction of RF department and research trend of RFIC in Vietnam, Tuan Khanh Nguyen, ICDREC, HCMC, Vietnam
15:50 PM - 16:10 PM	Thermoelectric properties of Indium, Gallium-doped ZnO thin films, Bach Thang Phan, University of Science, VNU, HCMC, Vietnam
16:10 PM - 16:30 PM	Closing address



A FULL-SWING 10-BIT CMOS CYCLIC D/A CONVERTER WITH A CAPACITOR-SHARING TECHNIQUE

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This paper describes a CMOS cyclic Digital-to-Analog Converter (DAC) for Automatic Test Equipment (ATE). In the middle of ATE, many kinds of DC reference voltages must be generated by DAC channels. In order to satisfy the DAC requirements, a small-area, a full-swing, and a high-resolution beyond 10-bit are needed. Therefore, a cyclic type DAC with a capacitor-sharing technique is proposed. Further, a full-swing output buffer is also discussed. The proposed DAC has been fabricated with 0.18 μ m, 1-poly, and 5-metal CMOS process. The effective chip size is 0.28mm² and the power dissipation is about 350 μ W at 5V power supply. The measured result of SFDR is 63dB, when the input frequency is 1MHz at the sampling frequency of 10MHz. The measured INL is within 1.5LSB and DNL is within 1.0LSB.

In this paper, I would like to talk about a cyclic type DAC which has a really low power consumption and an extremely small chip area. Since an ATE needs many kinds of DAC in the chip, the DAC must have an extremely small chip area. In order to implement the requirements, a capacitor-sharing technique is proposed. Further, a full-swing performance is also provided to have a sufficient Signal-to-Noise Ratio (SNR).

Acknowledgement:

This work was supported by the MOTIE (Ministry of Trade, Industry, and Energy) Korea, under the NGPEP (New Growth Power Equipment Project) program supervised by the KEIT (Korea Evaluation Institute of Industrial Technology), and Exicon Co. Ltd. The CAD tools were supported by IC Design Education Center (IDEC), Daejeon, Korea.

Minkyu Song received the B.S. and M.S., and Ph.D. degree in Electronics Engineering from Seoul National University, Korea in 1986, 1988 and 1993, respectively. From 1993 to 1994, he was a researcher at Asada Lab., VDEC, University of Tokyo, Japan where he worked in the area of low power VLSI design. From 1995 to 1996, he was a researcher in the CMOS Analog Circuit Design Team of Samsung Electronics, Korea. Since 1997, he has been a Professor at University of Dongguk, Korea. He is a member of IEEE and IEIE. His major interest is design of CMOS analog circuits, mixed-mode circuits, and low power digital circuits.



A LOW POWER SERDES FOR WIRELESS CHIP-TO-CHIP COMMUNICATION

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A low-power multi-Gbps serializer/deserializer (SerDes) with a phase interpolator (PI) based clock and data recovery (CDR) circuit for high-speed and short-range wireless chip-to-chip communication is presented. The SerDes performs 4:1 muxing and 1:4 demuxing functions. The PI-based CDR uses an 8-phase delay-locked loop (DLL) to produce a set of evenly spaced reference clock phases. The phase vernier, then transforms the 8-phases to sampling clocks for the sampler, which performs $2\times$ oversampling to recover the data from the input signal. Implemented in a 65nm CMOS process, the proposed SerDes achieves a data rate of 10Gbps and a recovered peak-to-peak clock jitter of 36.25ps. The 10Gbps SerDes occupies an active area of 0.095mm² and dissipates 88mW.

Jongsun Kim received his Ph.D. degree in Electrical Engineering from the University of California, Los Angeles (UCLA) in 2006 in the field of Integrated Circuits and Systems. He was a postdoctoral fellow at UCLA from 2006 to 2007. From 1994 to 2001 and from 2007 to 2008, he was with Samsung Electronics as a senior research engineer in the DRAM Design Team, where he worked on the design and development of Synchronous DRAMs, SGRAMs, Rambus DRAMs, DDR3 and DDR4 DRAMs. Dr. Kim joined the School of Electronic & Electrical Engineering, Hongik University in March 2008. Professor Kim's research interests are in the areas of high-performance mixed-signal circuits and systems design. His current research areas include high-speed and low-power transceiver circuits for chip-to-chip communications, clock recovery circuits (PLLs/DLLs/CDRs), frequency synthesizers, signal integrity and power integrity, ultra-low-power memories, power-management ICs (PMICs), RF-interconnect circuits, and low-power memory interface circuits and systems.



A STUDY OF MM-WAVE CIRCUITS BASED ON META-MATERIAL

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Meta-material is artificial structure having the property that does not exist in nature, it enables to realize radio wave characteristics which are impossible in practical like negative permittivity or negative permeability. So, we adopt meta-material for analog circuit design to get the improved characteristics of RF circuits. I will present the design approach using meta material in RF circuit design and show the research result using meta-material in mm-wave circuits.

Yong Moon received the B.S., M.S., and Ph.D. degrees from the Department of Electronics Engineering, Seoul National University, Seoul, Korea, in 1990, 1992 and 1997, respectively. From 1997 to 1999, he was with LG Semicon Co., Ltd., where he contributed to senior research engineer in analog circuit design group. Since 1999, he has been with Soongsil University, Seoul, Korea, where he is a professor in School of Electronic Engineering. His research interests include PLL, low-power circuit, mixed signal IC and RF circuits.



BATTERY LIFETIME AND PSNR QUALITY-SCALABLE VIDEO TRANSMISSION FOR MOBILE MULTIMEDIA SYSTEMS

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A battery lifetime and PSNR quality-scalable video transmission is proposed. Video bit stream is intentionally encoded at lowered bitrate, and it is intermittently transmitted to exploit battery recovery effect. Battery lifetime is extended significantly with PSNR quality degradation given by user. Both battery lifetime and PSNR quality are precisely estimated and easily controlled by adjusting encoding bitrate and battery duty ratio. Battery lifetime extension is fully scalable with PSNR quality degradation, and vice versa. Measured battery lifetime was significantly extended at the cost of small PSNR degradation.

Seongsoo Lee received the B.E., M.S. and Ph.D. degrees in Electrical Engineering from Seoul National University, Korea, in 1991, 1993, and 1998, respectively. He was a Research Associate at University of Tokyo, Japan from 1998 to 2000. He was a Research Professor at Ewha Womans University, Korea from 2000 to 2002. Since 2002, he has worked at the School of Electronic Engineering at Soongsil University, Korea, where he is currently a Professor. His research interests include low-power SoC, digital signal processing SoC, and multimedia SoC.



MEMRISTOR CROSSBAR CIRCUITS FOR ENERGY-EFFICIENT PATTERN RECOGNITION

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The memristors that had been mathematically predicted by L. O. Chua in 1971 as the fourth basic circuit element were experimentally found by HP researchers in 2008. Since the first prediction of memristors, they have been considered to be useful in future neuromorphic computing systems. Particularly, the nonlinear charge-flux relationship in memristors can be used in mimicking synaptic plasticity of biological neuronal systems such as human brains. In addition to this non-linear relationship, memristor crossbar array is thought to be suitable to realize brain-like architecture, because memristor crossbar architecture can be very dense and 3-dimensional like brain architecture. One of important advantages in neuromorphic systems is higher energy efficiency compared to the conventional Von Neumann systems. Hence, low-power consumption in memristor crossbar circuit is very crucial in realizing the useful neuromorphic systems for practical applications, such as image and speech recognition.

In this presentation, I would like to talk about memristor crossbar circuits which can be energy-efficient in bio-inspired pattern recognition. Here, I discuss a couple of matters that are critical to memristor circuits such as sneak-path leakage, energy efficiency, read voltage margin, etc. And, based on these critical problems, I try to suggest new crossbar architecture that consumes smaller amount of energy than the previous crossbar circuits.

Acknowledgement:

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Kyeong-Sik Min received the B.S. degree in Electronics and Computer Engineering from Korea University, Seoul, Korea, in 1991, and the M.S.E.E. and Ph.D. degrees in Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1993 and 1997, respectively. In 1997, he joined Hynix Semiconductor Inc., where he was engaged in the development of low-power and high-speed DRAM circuits. From 2001 to 2002, he was a research associate at University of Tokyo, Tokyo, Japan, where he designed low-leakage memories and low-leakage logic circuits. In September 2002, he joined the faculty of Kookmin University, Seoul, Korea, where he is currently a Professor in the School of Electrical Engineering. He was a visiting professor at University of California, Merced, from Aug. 2008 to July 2009. Prof. Min served on various technical program committees such as Asian Solid-State Circuits Conference (A-SSCC), International SoC Design Conference (ISOCC), and Korean Conference on Semiconductors (KCS). He and his students received IDEC CAD & Design Methodology Award (2011), IDEC Chip Design Contest Award (2011), and IDEC Chip Design Contest Award (2012). He is a member of Institute of Electrical and Electronics Engineers (IEEE), Institute of Electronics Engineers of Korea (IEEK), and Institute of Electronics, Information, and Communication Engineers (IEICE) in Japan. His research interests include low-power VLSI, memory design, and power IC design.



A SUCCESSFUL MODEL IN BUILDING-UP THE SEMICONDUCTOR INDUSTRY AT VIETNAM

Hitoshi Sugihara and Tuong Hai Pham

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Conducting the feasibility study from 2003 and established in 2004 even when LSI design was still an unfamiliar word with most of Vietnamese people, but Renesas Design Vietnam (RVC) was targeted as a full range design center at Vietnam. This presentation share to audiences the background and expectation on the foundation of RVC, the challenge issues and development strategies, the local workforce and training scheme, the success and efforts, contribution, that RVC experiences through more than 10 years of development and growth. We close the presentation by an active message to engineers who interest on semiconductor industry and wish to contribute to the prosperity of the region.

Hitoshi Sugihara received the B.S. degree in Informational Technology and Computer Engineering from Gunma University, Japan, in 1983. In 1983, he joined Hitachi Co., Ltd., Tokyo, Japan, where he was engaged in the development of MOS device modeling and circuit simulator. From 1993 to 2009, he developed a Analog and Digital Mixed Signal LSI for RF in Renesas Technology Co., Ltd, Tokyo, Japan. From 2010 to 2012, he developed a CPU core of MCU in Renesas Electronics Co., Ltd, Tokyo, Japan. From 2013, he is a president of Renesas Design Vietnam Co., Ltd which is the first major High-Tech Semiconductor R&D Company certified by Vietnamese government , Ho Chi Minh City, Vietnam. He has 3 patents and 5 IEEE papers (ICCAD, IEDM) which are related to MOS device modeling and circuit simulation algorithm.

Tuong Hai Pham received the B.S. in Computer Science and Engineering at Ho Chi Minh City University of Technology (HCMUT), Vietnam, in 1986. He received D.E.A and Ph.D. in Fundamental Informatique and Parallelism at Paul Sabatier University, Toulouse, France, in 1994 and 1997 respectively. From 1986 to 1993, he was at the Informatique Center of HCMUT, working on design of telecommunication and network used in provinces in the south of Vietnam. He then joined the Faculty of Information Technology of HCMUT since 1998. He was the Head of Computer Engineering Department from 1998 to 2002 and the Dean of the Faculty of Information Technology from 2002 to 2007. He joins Renesas Design Viet Nam Co., Ltd. from 2008 as Advisor and in charge of the training for engineers.



STUDY OF THE RESISTIVE SWITCHING EFFECT IN CHROMIUM OXIDE THIN FILMS BY USE OF CONDUCTIVE ATOMIC FORCE MICROSCOPY

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Reversible resistive switching of Cr_2O_3 films was studied by use of conductive atomic force microscopy. Resistive switching in Cr_2O_3 films occurs as a result of Ag filament paths formed during electrochemical redox reactions. A large memory density of 100Tbit/sq. inch was achieved with a small filament diameter of 2.9nm under the action of a compliance current of 10nA. A fast switching speed of 10ns, high scalability, and low set/reset currents suggest that Cr_2O_3 -based resistive memory is suitable for nanoscale devices.

Acknowledgement:

This work was funded by National Foundation of Science and Technology Development of Vietnam (NAFOSTED – 103.02-2012.50), The Exchange Fellowship Programme under ASEAN-ROK Academic Exchange Programme 2014, and the Basic Science Research Program through National Research Foundation of Korea (2009-0092809).

Bach Thang Phan is Vice Dean of Faculty of Materials Science at University of Science (US), VNUHCM. He received the BS degree in Physics (Applied Physics) from US, VNUHCM, in 2001. He received the PhD degree in Electronic Materials in SungKyunKwan University, South Korea (2009) and he became an Associate Professor in Physics at US, VNUHCM (2015). His research focuses on nanostructured materials applied in Resistive memory (RERAM), Memristive biosensor and thermoelectric conversion.



A NEW MULTIPLICATION ARCHITECTURE WITH MIXED DATA FORMAT FOR DSP APPLICATIONS

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The modern digital logic technology does not yet satisfy the speed requirements of real-time DSP circuits due to synchronized operation of multiplication and accumulation. This operation degrades DSP performance. Therefore, the double-base number system (DBNS) has emerged in DSP system as an alternative methodology because of fast multiplication speed and hardware simplicity.

In this paper, authors propose novel multiplication architecture. One operand is an output of a flash analog-to-digital converter (ADC) in DBNS format, while the other operand is a coefficient in the IEEE standard floating-point number format. The DBNS digital output from ADC is produced through a new double base number encoder (DBNE). The multiplied output is in the format of the IEEE standard floating-point number (FPNS). The proposed circuits process multiplication and conversion together. The speed and power consumption improvements of DBNE are 39.4% and 50%, respectively compared to the fastest FAT tree encoder in 0.18 μ m CMOS technology. Compared to a typical multiplier that uses the FPNS, the proposed multiplier also consumes 45% less gates, and 44% faster than the FPNS multiplier on Spartan-3 FPGA board. The design is verified with FIR filter applications.

Minh Son Nguyen is the Dean of Faculty of Computer Engineering in University of Information Technology (UIT), Vietnam. His research fields are Wireless Embedded System, System on Chip and VLSI Design. Dr. Nguyen is a member of Program Committee of HCM City Department of Science and Technology and Vietnam National University at HCM City in research fields of Integrated Circuit Design. Also he is member of Technical Program Committee of ATC, ACOMP Conferences. Dr. Nguyen had 10-year experiences in Embedded System while served in Metran Company (HCM City), Mooha Digital Company (Seoul) and PowellTechwin Company (Ulsan). He had 5-year experiences in research of VLSI Design and SoC as well. Now, he is a leader of research groups in IoTs and AC-Directed LED Driver IC. Dr. Minh Son Nguyen received his Ph.D. in Computer Engineering from University of Ulsan, Korea.



ICDREC AND THE DEVELOPMENT OF IC DESIGN IN VIETNAM

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The IC design industry in Vietnam has started since 2007, with the successful tape-out chip SigmaK3, an 8-bit microcontroller, designed by ICDREC. After the success of some other chips designed by ICDREC, governmental policies were created to help developing the high technology in general and IC design industry in particular at national level. Especially, Ho Chi Minh City has launched the program of Semiconductor Industry Development since 2013. Besides, big corporations in IC design have also set up their R&D center in Ho Chi Minh City. These are big motivation for the research activities in IC design in Vietnam in the near future.

In this presentation, I would like to talk about the story of ICDREC's success as a pioneer in Vietnam. I introduce the organization model of ICDREC, its key achievements during the past 8 years, on-going research projects and strategic products. Some typical collaborations are also presented to discuss on future joint research activities.

Quang Vinh Ngo is the vice director at ICDREC, Vietnam National University - Ho Chi Minh City (VNU-HCM). He is also the Ph.D. student at the University of Technology where he graduated from Bachelor and Master program at the Faculty of Electrical and Electronics. His research interests include chip multiprocessor architecture, high performance microprocessor design, parallel computing and parallel architecture design. He is a reviewer for conferences such as Solid State Systems Symposium – VLSIs and Semiconductor Related Technologies (4S), International Conference on Advanced Technologies for Communications (ATC). He serves on the technical program committee of 4S 2014 and 2016 Symposium. His team won the highest prize at Vietnam Talent Awards 2009 with the 8 bit microprocessor chip VN801.



DUAL POWER GATING TECHNIQUES FOR SMALL LEAKAGE ENERGY LOSS IN LOW POWER APPLICATIONS

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We reconsider the dual power gating techniques to reduce the leakage power consumption in sleep mode and retention mode. By turning-off both PMOS header and NMOS footer, dual power gating can fairly be compared to recent power gating techniques to claim that the dual power gating is a very effective technique to mitigate the leakage energy loss from active to sleep mode. Modified dual power gating technique is also used to recycle charge lost at moment from active to retention mode. We compare the advantages of leakage power consumption with recent power gating techniques through the 32-bit CLA circuit and ISCAS-85 benchmark.

Minh Huan Vo received the B.S. and M.S.E.E. degrees in Electronics and Communication Engineering from the Ho Chi Minh City University of Technology, Vietnam in 2005 and 2007 and Ph.D. degree in Electronics Engineering from Kookmin University, Seoul, Korea in 2013. He is currently working as a lecturer at the Faculty of Electrical and Electronics Engineering, University of Technology and Education, Ho Chi Minh City, Vietnam. His current research interests include low power design optimization and neuromorphic computation using emerging technology like memristive devices.



INTRODUCTION OF RF DEPARTMENT AND RESEARCH TREND OF RFIC IN VIETNAM

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The RF department is a young one which have included many passion and creativeness researcher. We focus on the study and design of system and circuit for satellite and short distance communication operating at RF frequencies. We also develop various types of IP (intellectual property) related RFIC and modules which is cooperated with other department in ICDREC. The researches in these fields need a wide range of knowledge including CMOS, microwave and antenna theory, wireless communication system analysis and design, RF transceiver architectures, mixed-signal and Analog/RF simulation, electromagnetic modeling and simulation, measurement of RF and microwave components. The current projects which have been researching of us at ICDREC can be showed such as: HF and UHF RFID tag, GPS, UHF Transceiver. Besides, researches and designs of small size, low power and improved performance, multiband and multi channels transceiver are especially focused for WSN (Wireless Sensor Network) and IoT (Internet of Things) in the near future. We have 6 members who got 2 -5 years working experience and all of us was postgraduate degree from Ho Chi Minh City University of Technology, Ho Chi Minh City University of Science, or Ho Chi Minh City International University. We have the basic knowledge about Analog and RFIC design and experience of using Cadence, ADS, Systemvue, IE3D and AppCad... The new one must spend a lot of time to study and research books and IEEE papers related Microwave engineering, CMOS analog and RF design. After that, they must understand and design the system to build the specification of each block. The design schematic, layout and run post-layout simulation also take a lot of time of the researcher. Finally, the chip must be measured by many necessary equipment to evaluate and optimize the circuit again and again. Most of equipment at ICDREC was supplied from Keysight and Tektronix which can be showed as: Vector Network Analyzer-VNA 8.5GHz, Oscilloscope DSO7054B, Spectrum Analyzer N9010A, Noise Source N4001A, RF Signal Generator, Digital Precision Multimeter...The department also have program training short courses and advice the thesis for students and researchers. We have a good communication with many University and some department of government and companies in Vietnam. We usually receive the advices from Professor Dang Luong Mo who was the consultant of Vietnam National University- HCMC, and Professor Bui Ngoc Chau who was director of Identic (Switzerland). Moreover, we got a lot of experiences on using the PDK from TSMC such as 180 nm and 130 nm. We are going to use the SOTB process which will be supplied by Renesas for our project in the next time.

Tuan Khanh Nguyen received the M.S. degrees in electrical engineering from HCM University of Technology. Now he is the manager of RF department of ICDREC. His research interests include transceiver architectures, PA, VCO & PLL design.

Kim Vu Tran received M.S degrees in electrical engineering at HCMUT. His research interests include system design, LNA, Mixer and Polyphase Filter.



THERMOELECTRIC PROPERTIES OF INDIUM, GALLIUM-DOPED ZNO THIN FILMS

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In this paper, we investigated the effect of single and multi-dopants on crystallinity and electrical properties of the host ZnO films. While incorporation of single Ga in the ZnO films improves electrical properties, multi-dopant doping (Ga and In) introduce degradation of electrical properties. The variation of electrical properties is discussed in term of film crystallinity, which is controlled by dopant radius. Small amount of In dopant with large radius may introduce localized regions in the host film, where localized carriers and lowered carrier mobility.

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This work was funded by National Foundation of Science and Technology Development of Vietnam (NAFOSTED).

Bach Thang Phan is Vice Dean of Faculty of Materials Science at University of Science (US), VNUHCM. He received the BS degree in Physics (Applied Physics) from US, VNUHCM, in 2001. He received the PhD degree in Electronic Materials in SungKyunKwan University, South Korea (2009) and he became an Associate Professor in Physics at US, VNUHCM (2015). His research focuses on nanostructured materials applied in Resistive memory (RERAM), Memristive biosensor and thermoelectric conversion.



LIST OF ATTENDEES

Minkyu Song (Dongguk University, Seoul, Korea)
Jongsun Kim (Hongik University, Seoul, Korea)
Yong Moon (Soongsil University, Seoul, Korea)
Seongsoo Lee (Soongsil University, Seoul, Korea)
Kyeong-Sik Min (Kookmin University, Seoul, Korea)
Quang Vinh Ngo (ICDREC, HCMC, Vietnam)
Tuan Khanh Nguyen (ICDREC, HCMC, Vietnam)
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POSTER

THE RISE OF FPGA DEMAND IN AUTOMOTIVE INDUSTRY

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The recent breakthrough innovation in automotive has escalating demand for FPGA, make automotive industry become the third largest FPGA application segment after telecom and industrial. Xilinx, Altera and Microsemi have recently introduced their Automotive-grade FPGA devices into the market. The main application areas in automotive that make extensive use of FPGA devices include Advanced Driver Assistance System (ADAS), Infotainment and Driver Information, Hybrid-Electric vehicles (HEV), Electric vehicles (EV), and In-Vehicle networking. This presentation will discuss what factors are driving the adoption of FPGA in automotive and how the FPGA is applied in the above application.

The Dai Duong Nguyen received B.Eng. and M.S. in Telecommunications and Electronics at Ho Chi Minh City University of Technology in 2005 and 2007 respectively. He joined Altera Vietnam in 2007 as Design Engineer and involved in the development and maintenance process of DSP IP cores. In 2009, he joined IC Design and Research Education Center – VNU where he was in charge of managing the IP Team. From 2012 to 2014, he worked at Viettel Research and Design Institute, contributed to the IC design project. He joined Robert Bosch Engineering Vietnam from 2015 as Software Architect specialized in FPGA domain.



APPLICATIONS OF MEMRISTOR IN NEURAL NETWORK

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Neuromorphic circuits with memristor are proposed for speech and character recognition in this research. In character recognition, we propose the bridge memristor circuit to generate synaptic weights including positive, negative and 0 values in the range $[-1; 1]$. We use two kinds of square pulse: a large width pulse is used to program synaptic weights and a small width is used to compute the weighting and inputs. Each digit from 1 to 5, sampled by 10 times, forms a 5×4 matrix to show simulation results. In speech recognition, we propose a crossbar circuit with binary memristor. The proposed binary memristor crossbar can recognize five vowels with 48 4-bit-input channels. The crossbar circuit is designed base on neural network. The proposed crossbar is tested and verified to be able to recognize 94.8% of the tested samples.

Thanh Ngoc Le received the B.S. degree in Faculty of Electrical and Electronics Engineering from the Ho Chi Minh City University of Technology, Vietnam in 2014. He is currently working toward M.S degree in Electronics Engineering at Ho Chi Minh City University of Technology, Viet Nam. His research interests include analysis of memristor and memristive system, neuromorphic computing systems.

Van Tien Nguyen received the B.S. degree in Faculty of Electrical and Electronics Engineering from the University of Technology and Education, Ho Chi Minh City, Vietnam in 2014. He is currently working toward the M.S degree in Electronics Engineering. His current research interests include memristor and memristor - based crossbar for neuromorphic computing systems.



A DIGITAL FILE TRANSMISSION SYSTEM WITH COMPUTER USING VISIBLE LIGHT COMMUNICATION

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Visible Light Communication (VLC) gets more attention in recent years. A digital file transmission system with computer is designed and tested in this work. We design a file transmitter which we can transfer the selected files through DE-1 FPGA kit. Commercially available LED and photodiode are used. The Manchester modulation is chosen for encoding the bit data. We analyzed the maximum baud rate, distance range and delay between transmitter and receiver to optimize the system. The demonstration results show the system is stable and qualified.

Huu Duc Le and **Duc Long Chu Nguyen** are final year student in Faculty of Electrical and Electronics Engineering from the University of Technology and Education, Ho Chi Minh City, Vietnam He is currently working toward the Engineer degree in Electronics Engineering. His current research interests include FPGA applications, VLC communication.



SCHEDULING ENERGY USAGE BASED ON DYNAMIC FREQUENCY SCALING TECHNIQUE IN LIMITED POWER BUDGET APPLICATIONS

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In this work, we schedule the energy consumption based on the dynamic frequency scaling technique where battery applications have the limited power budget. The three levels of 50MHz, 25MHz and 5MHz frequency operation are planed according to the sensing current to extend the battery life time. The Ping-pong game application is applied to 2500mAh battery source for experiment tests.

Van Nhut Nguyen is final year student in Faculty of High Quality Training from the University of Technology and Education, Ho Chi Minh City, Vietnam He is currently working toward the Engineer in Electronics Engineering. His current research interests include time-to digital converter, temperature sensor.



THE MERGED CLOCK GATING ARCHITECTURE FOR LOW POWER DIGITAL WATCH APPLICATION ON FPGA

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In this work, we propose a merged clock gating architecture to design low power digital watch. We compare the proposed technique with the conventional clock gating and no-clock gating technique in term of total power consumption. The simulation results in Spartan-3E show that the proposed can save 5%, 28%, 57%, 60%, 60,5% compared to the no-clock gating and 1.19%, 1.85%, 11.83%, 14.76%, 15.67% compared to the conventional clock gating technique in frequency operation of 100MHz, 1GHz, 10GHz, 100GHz and 1THz, respectively. Moreover, the proposed technique can reduce to 25% and 5% compared to the no-clock gating and the conventional clock gating in term of the temperature operation, respectively. The number of LUT also decreases to 175 instead of 179 in the other techniques.

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A 5PS RESOLUTION CMOS TEMPERATURE SENSOR USING 2-STAGE VERNIER TECHNIQUE IN 45-NM NODE

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This paper presents the architecture and performance of a high-resolution time-to-digital converter (TDC) based on 2-stage Vernier delay line. The temperature sensor generates a pulse with width proportionally to the temperature by using temperature dependent delay line and temperature insensitive delay line. Pulse width is converted to a corresponding digital code by time-to-digital (TDC) converter. Simulation and experimental results using an analog design environment Cadence tool indicate that the method can be employed to calibrate high-resolution TDCs with high accuracy. The time-to-digital converter circuit was designed and implemented in 45nm CMOS technology and achieves a resolution less than 5ps. We also compare the resolution with the recent published results.

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ADJUSTING THRESHOLD VOLTAGE FOR LOW POWER CONSUMPTION SRAM IN RETENTION MODE

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The transistor threshold voltage is nonlinearly proportional to the source-body voltage and becomes saturated with the larger source-body voltage. In retention mode, instead of applying a certainly large voltage level to virtual ground or single virtual power of SRAM cells to save power as usual, we divide this voltage level to apply to both virtual power and ground to save more power loss. By doing so, technique of the virtual ground and power reduction (VGPR) can save to 44.3% and 72% leakage power compared to virtual ground reduction (VGR) and virtual power, respectively. In active time, power-delay product of VGPR is little smaller than VGR and VPR although the delay of VGPR is higher than the others.

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FLEXIBLE COLOR CONTROL ON VISIBLE LIGHT COMMUNICATION SYSTEM

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To improve the bandwidth, speed, communications in restricted areas of radio and especially the communication, but to ensure the health of the person, The research team proposed the communication technique by visible light, with desired both lighting and communication, the use of light with colors Red, Green and Blue, we can create the desired color. In this paper, the research team proposed control method used color and brightness LED RGB technique synchronized lights, the system uses 3 switch to control 7 state color, corresponding to the bandwidth 7 and at different speeds. This paper presents the results of simulating the blocks of modulation and demodulation method respectively was proposed, with 50Mhz clock, the result after the simulation is loaded on chip FPGA, in a model experiments to test the accuracy of the program.

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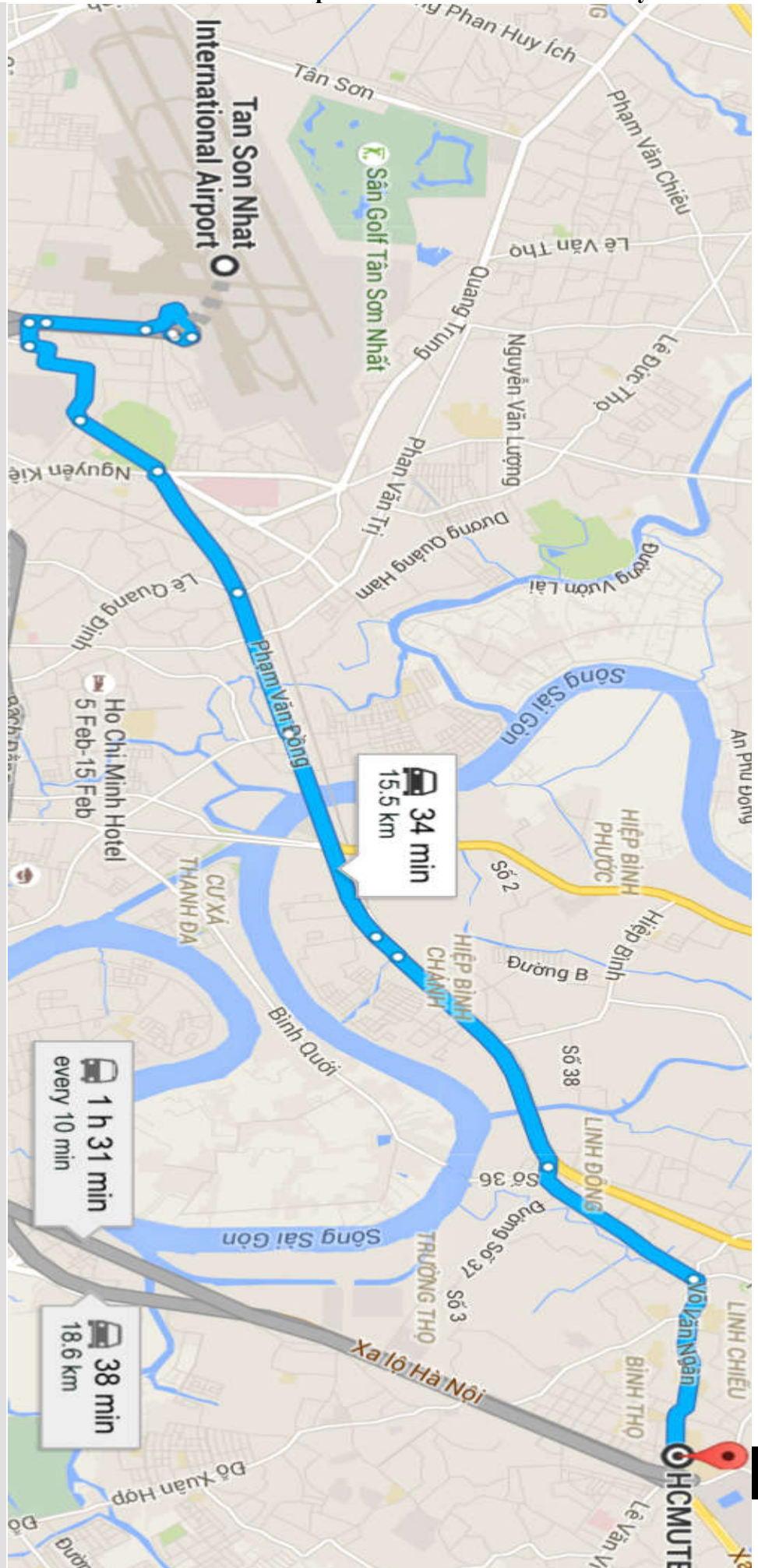


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